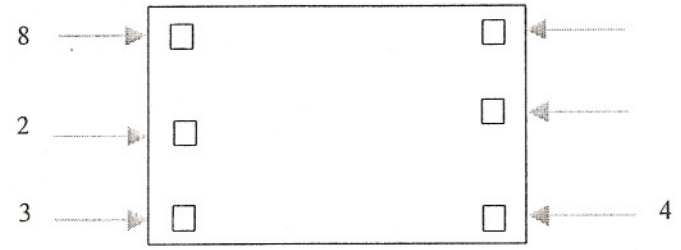
Sierra Components, Inc.

2222 Park Place Building 3 Suite E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD	FUNCTION
1	NC
2	V INV
3	V NON-INV
4	–VCC
5	NC
6	VOUT
7	+VCC
8	RP

The information for this layout is believed to be correct at the time of issue. Please verify your requirements against this information, prior to commencement of any assembly process, as no liability for omission or error can be accepted.
All devices supplied against this padlayout will comply with the physical size detailed below.
Pad positions shall obey the following rules:

1. Pad functions shall not change sequence and shall agree with the above definitions.
2. No pad function shall completely change side(s) from that shown above.
3. No pad function shall move by more than 1mm from the position shown.
4. No pad function shall move from a corner, and another move into that corner, even if the above constraints are met.

Topside Metal: Al
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:	**DIE SIZE (Mils): 45 x 32**	**DATE: 3/16/00**
MFG: Comlinear	**THICKNESS:**	**P/N: CLC505AMC**